Claims Appendix
(Showing Support for Claims)

1. - 4. (withdrawn)

5. A memory controller ([0084]; FIG. 1, 100), comprising:

a plurality of data pads and strobe pads ([0041]; FIG. 2, DQS0, DQS18, DQ0-DQ7), wherein data is read and written at each of said data pads in sync with a strobe that is received at or generated by a corresponding one of said strobe pads;

for each data pad (FIG. 18, DQ4), receiver circuitry comprising P storage elements ([0114-0116]; FIG. 18, 1802, 1804, 1806, 1808), wherein i) in a first mode, data bits stored by the P storage elements are multiplexed to generate a single data stream ([0117-0121]; FIG. 18, INH), and ii) in a second mode, data bits stored in the P storage elements are multiplexed to generate at least two data streams ([0122-0129]; FIG. 18, INH, INL); and

for each strobe pad (FIG. 19, DQS18), receiver circuitry comprising a counter ([0136-0158]; FIG. 19, 1900) to count received strobe edges; wherein particular counts (FIG. 19, S1-S4) of strobe edges received at a particular strobe pad cause data to be received by particular ones of the P storage elements associated with data pads corresponding to the particular strobe pad.

6. The memory controller of claim 5, wherein each of said storage elements is a latch ([0114]).

7. The memory controller of claim 5, wherein each of said storage elements is a flip-flop ([0120]).

8. The memory controller of claim 5, wherein each of said counters is a rollover counter which produces said count as a P bit, one-high count ([0138]).

9. The memory controller of claim 5, wherein P=4 ([0138]).

10. The memory controller of claim 5, wherein the at least two data streams consist of even and odd data streams ([0129]).

11. The memory controller of claim 5, further comprising:

a clock generation circuit ([0071], [0077-0081]; FIG. 7, 700; FIG. 8) to generate strobes at said strobe pads (FIG. 8, DQS18) at a 1x rate when the memory controller is configured in said first mode, or at an Mx rate when the memory controller is configured in said second mode;

for each data pad (FIG. 8, DQ4), driver circuitry ([0072-0074]; FIG. 8, 800) to alternately couple ones of a corresponding subset of N data propagation circuits to the data pad, thereby driving a merged data stream to the data pad; and

circuitry ([0061], [0064-0067]; FIGS. 4, 6 & 8, 410, 412, 610, 612) to, i) in said first mode, provide like data input streams to each of the N data propagation circuits associated with a given data pad, and ii) in said second mode, provide different data input streams to each of the N data propagation circuits associated with a given data pad.

12. The memory controller of claim 11, wherein for each data pad, said driver circuitry comprises N sequentially clocked flip-flops ([0062]; FIG. 5, 500, 502) which respectively receive and output data from the N data propagation circuits.

13. The memory controller of claim 11, wherein for each data pad, said driver circuitry comprises a multiplexer ([0064]; FIG. 6, 606) which receives and sequentially outputs data from the N data propagation circuits.

14. The memory controller of claim 11, wherein for each data pad, said driver circuitry comprises N tri-statable paths ([0062]; FIG. 5, 504, 506) which respectively receive and sequentially output data from the N data propagation circuits.

15. The memory controller of claim 5, further comprising a memory ([0087]; FIG. 11, 1100) to store indications of data/strobe ratios that are required to access memory devices that are coupled to said data and strobe pads of the memory controller; wherein, for a data transmission initiated with a particular one of the memory devices, a number of said data pads is dynamically associated with a number of said strobe pads, in response to a corresponding indication of a data/strobe ratio stored in the memory.

16. A computer system (FIG. 1, 124), comprising:

a CPU (FIG. 1, 102);

a memory controller ([0084]; FIG. 1, 100) coupled to said CPU; and

a number of memory devices (FIG. 1, 104) coupled to said memory controller;

wherein said memory controller comprises:

a plurality of data pads and strobe pads ([0041]; FIG. 2, DQS0, DQS18, DQ0-DQ7) coupled to said memory devices, wherein data is read and written at each of said data pads in sync with a strobe that is received at or generated by a corresponding one of said strobe pads;

for each data pad (FIG. 18, DQ4), receiver circuitry comprising P storage elements ([0114-0116]; FIG. 18, 1802, 1804, 1806, 1808), wherein i) in a first mode, data bits stored by the P storage elements are multiplexed to generate a single data stream ([0117-0121]; FIG. 18, INH), and ii) in a second mode, data bits stored in the P storage elements are multiplexed to generate at least two data streams ([0122-0129]; FIG. 18, INH, INL); and

for each strobe pad (FIG. 19, DQS18), receiver circuitry comprising a counter ([0136-0158]; FIG. 19, 1900) to count received strobe edges; wherein

particular counts (FIG. 19, S1-S4) of strobe edges received at a particular strobe pad cause data to be received by particular ones of the P storage elements associated with data pads corresponding to the particular strobe pad.

17. The computer system of claim 16, wherein each of said counters is a rollover counter which produces said count as a P bit, one-high count ([0138]).

18. The computer system of claim 16, further comprising:

a clock generation circuit ([0071], [0077-0081]; FIG. 7, 700; FIG. 8) to generate strobes at said strobe pads (FIG. 8, DQS18) at a 1x rate when the memory controller is configured in said first mode, or at an Mx rate when the memory controller is configured in said second mode;

for each data pad (FIG. 8, DQ4), driver circuitry ([0072-0074]; FIG. 8, 800) to alternately couple ones of a corresponding subset of N data propagation circuits to the data pad, thereby driving a merged data stream to the data pad; and

circuitry ([0061], [0064-0067]; FIGS. 4, 6 & 8, 410, 412, 610, 612) to, i) in said first mode, provide like data input streams to each of the N data propagation circuits associated with a given data pad, and ii) in said second mode, provide different data input streams to each of the N data propagation circuits associated with a given data pad.

19. The computer system of claim 16, further comprising a memory ([0087]; FIG. 11, 1100) to store indications of data/strobe ratios that are required to access memory devices that are coupled to said data and strobe pads of the memory controller; wherein, for a data transmission initiated with a particular one of the memory devices, a number of said data pads is dynamically associated with a number of said strobe pads, in response to a corresponding indication of a data/strobe ratio stored in the memory.